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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/842,312	04/25/2001	Andrew C. Sturges	S01022/80655 (JHM/EJR)	6679

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EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	17

DATE MAILED: 03/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/842,312	STURGES ET AL.	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *38-48 and 50-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *38-48 and 50-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 38-48 and 50-57 are presented for examination. Claims 58-59 are newly presented for examination.

2. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> (c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

3. This application currently names joint inventors. In considering patentability of the claims under 35 USC § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 USC § 102(f) or (g) prior art under 35 USC § 103.

4. Claims 38-48 and 50-59 are rejected under 35 USC § 103 as being unpatentable over Cocke et al., U.S. Patent 3,577,189, in view of Bruckert et al., U.S. Patent 4,742,451.

Cocke et al. and Bruckert et al. were cited as prior art references in paper number 13, mailed July 29, 2003.

Cocke et al. taught (e.g. see figs. 1-7a) the invention substantially as claimed (as per claim 38), including a data processing ("DP") system comprising:

4.1. a computer system (fig. 1) comprising;

4.2. storage circuitry (a memory, inherently present, see also col. 5 lines 20-22) for holding a plurality of instructions (fig. 5) at respective storage locations (a memory inherently contains respective storage locations), the plurality of instructions including a first string of instructions (fig. 5, left side vertical line, $OP_{\alpha 1}$ through $OP_{\alpha 10}$, including "BRANCH" and "EXIT") including a set branch instruction ("BRANCH") indicating a target location (fig. 4a, col. 4 lines 64-67) within the storage circuitry at which a new instruction (right side vertical line, $OP_{\beta\#}$), not included in the first string (the right hand instruction string is not included in the left hand instruction string), is stored, the first string (left side) further including a subsequent instruction ($OP_{\alpha 4}$ through $OP_{\alpha 10}$, including "EXIT") that is subsequent in the first string to the set branch instruction (all

of $OP_{\alpha 4}$ through $OP_{\alpha 10}$, including "EXIT" are subsequent to "BRANCH");

4.3. execution circuitry to execute fetched instructions, including executing the set branch instruction (fig. 1a, 40, 62).

5. Cocke et al. did not teach instruction fetch circuitry having first and second instruction fetchers to fetch from the first and second strings in parallel, nor operation of the second instruction fetcher to fetch the new instruction in parallel with the first instruction fetcher fetching the subsequent instruction. However, Bruckert et al. taught a system (fig. 1) containing two instruction fetchers for fetching, respectively, a subsequent instruction and a new instruction (fig. 2a, 30, col. 2 lines 49-57 and col. 7 lines 16-34) upon detection of a branch instruction (col. 2 lines 34-39).

6. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined Bruckert et al.'s dual instruction fetching system with Cocke et al.'s set branch instruction system because of Cocke et al.'s teaching that the reason for using a set branch instruction is to accelerate processing of branches that otherwise cause delay (col. 1 lines 35-50) and Bruckert et al. teaches that by using a dual instruction fetcher system, both the taken and not taken paths of a branch will be fetched in parallel (col. 2 lines 33-67). Cocke et al.'s system will compliment Bruckert et al.'s system by providing early calculation of the effective address to which the branch will transition (col. 1 lines 45-50) thereby allowing Bruckert et al. second parallel instruction fetcher time to prefetch instructions along both paths of the branch, because as stated by Cocke et al. (col. 1 lines 27-50) branches cause delay if not processed early.

7. As to claim 39, Cocke et al. taught that the first string of instructions includes a condition instruction ("BRANCH") which defines a condition and defines that further instructions to be executed with include the new instruction only if the condition is satisfied (col. 2 lines 2-14).

8. As to claim 40, Cocke et al. taught that the first string of instructions further included an effect branch instruction ("EXIT") for implementing a branch to the location indicated by

the set branch instruction (col. 2 lines 14-28).

9. As to claim 41, Cocke et al. taught select circuitry responsive to execution of the effect branch instruction to cause the execution circuitry to execute the new instruction if the condition defined by the condition instruction is satisfied (col. 2 lines 20-28).

10. As to new claim 58, Bruckert et al. taught select circuitry operable to connect a selected one of the first and second instruction fetchers to the execution circuitry (col. 2 lines 56-68).

11. As to claim 42, Bruckert et al. taught that the instruction fetch circuitry comprised two instruction buffers, a first buffer connected to said execution circuitry to hold the further instructions to be executed (col. 2 lines 49-51), and a second buffer to hold a second string of instructions including the new instructions (col. 2 lines 52-56) wherein the computer system includes circuitry to copy the contents of said second buffer into said first buffer responsive to execution of said effect branch instruction (col. 2 lines 60-68).

12. As to claim 43, Bruckert et al. did not teach a third instruction fetch circuitry to implement predicted conditional instructions. However, branch prediction is notoriously well known in the prior art and official notice of such is hereby taken. Additionally, it has also been shown that merely duplicating parts of multiple effects is generally not given patentable weight (*St. Regis Paper Co. v Bemis Co.* 193 USPQ 8 (7th Cir. 1977). It would have been a simple matter of routine engineering for one of ordinary skill in the art to implement a third instruction fetcher within the system of Bruckert et al. for the purposes of handling predicted branch execution because doing so would allow for the system to be able to properly prefetch the required stream of execution before it was needed by the processor, enhancing performance of the system.

13. As to claim 48, Cocke et al. taught that the effect branch instruction ("EXIT") was located at a branch point after which said new instruction was to be executed (col. 2 lines 14-17 and 20-28).

14. As to claim 50, Cocke et al. taught that the computer system comprised a branch point

register for holding the branch point (fig. 1c, 54).

15. As to claim 51, Cocke et al. taught the computer system comprising a return register (fig. 1c, 54) for holding a return address being the address of the next instruction after said branch point, and wherein said set branch instruction identifies said return register to indicate the target location (col. 4 lines 64-67 and col. 5 line 67 to col. 6 line 7).

16. As to claim 44, Cocke et al. taught that the target location holds an address (fig. 5, EBA) of the new instruction (fig. 5, right side, $OP_{\beta\#}$) which is a first instruction of a string of new instructions to be fetched ($OP_{\beta\#}$ to $OP_{\beta7}$).

17. As to claim 45, Cocke et al. taught that the branch instruction identified a special register which holds an address from which a first instruction of a string of new instructions is to be fetched (col. 4 lines 64-68).

18. As to claim 46, Bruckert et al. taught a branch mode where the target location held and address of a memory location which held the address of the first instruction of the string of new instructions to be fetched (col. 5 lines 56-60).

19. As to claim 47, Cocke et al. taught decode circuitry (fig. 1a) for decoding said fetched instructions, the instruction fetch circuitry, decode circuitry, and execution circuitry being arranged in a pipeline (col. 1 lines 22-40).

20. As to claims 52-57 and new claim 59, they do not teach or define above the invention claimed in claims 38-48 50-51, and 58 and are therefore rejected under Cocke et al. in view of Bruckert et al. for the same reasons set fourth in the rejection of claims 38-48 50-51, and 58, supra.

21. In the remarks, applicant argues in substance:

21.1. That: "Bruckert et al. fails to disclose a computer system comprising ... an instruction fetcher operative, responsive to execution of said set branch instruction, to fetch a new instruction from a location indicated by a set branch instruction, in parallel to another instruction fetcher fetching a subsequent instruction."

This is not found persuasive because as detailed in the rejection, supra., Bruckert et al. does not teach such a set branch instruction. However, as is clearly seen from the rejection,

Cocke et al. does indeed teach just such a set branch instruction (fig. 5, "BRANCH") which functions as and performs all the functions of applicant's claimed set branch instruction. When Cocke et al.'s set branch ("BRANCH") instruction is combined with Bruckert et al.'s dual instruction fetcher system, Cocke et al.'s set branch instruction would instruct Bruckert et al.'s second instruction fetcher of the address from which it should begin fetching instructions in anticipation of the branch being taken.

22. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

23. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Richard Ellis
February 23, 2004

RICHARD L. ELLIS
PRIMARY EXAMINER